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2022BEE1192

INDIAN INSTITUTE OF TECHNOLOGY ROPAR

GE108: Basic Electronics

Mid-Semester Examination

Max. Marks: 50 Duration: 2 Hours

Question I: Consider the circuit shown in Fig.1 with one practical diode, one capacitor and one 5 V DC supply. Assume that conducting diode exhibits a constant voltage drop of 0.7 V. Sketch and label output voltage for input shown. Please present necessary calculation and simplify circuits to justify output voltage levels. [6 pts]

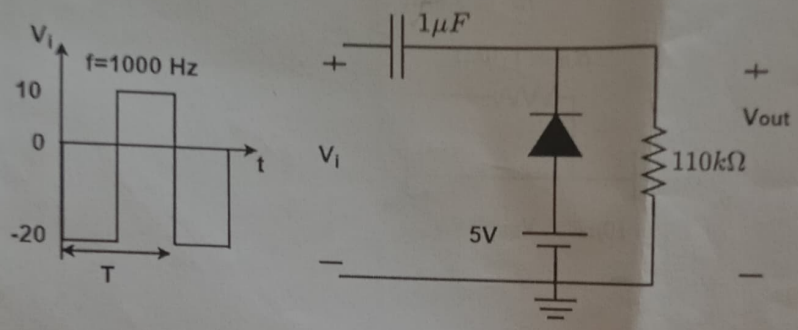

Fig.1: Diode circuit for Q-I

Question II: Consider the circuit shown in Fig.2 with one practical diode, two resistors and one 1V DC supply. Assume that conducting diode exhibits a constant voltage drop of 0.7 V. Sketch and label output voltage for input shown. [6 pts]

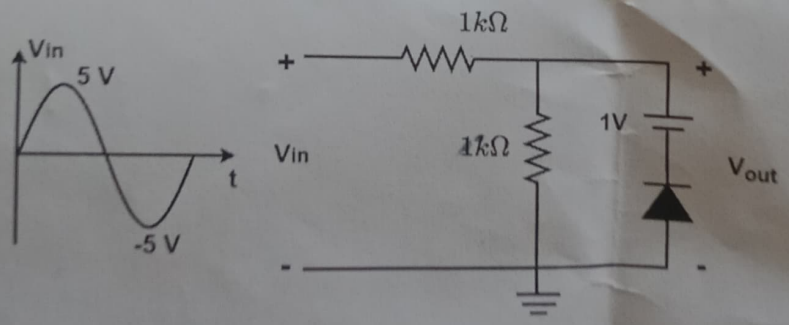

Fig.2: Diode circuit for Q-II

Question III: The BJT in the circuit of Fig. 3 has a β value of 200. Please answer the following questions:

(a) What is the name of the BJT configuration? [1 pt]

(b) What is the role of the R_B resistance in this circuit? [2 pts]

(c) Calculate the values of V_{CE} and I_C. What is the operating region of the BJT? [2 pts]

(d) Plot the quiescent (Q) point position on the load line for the above circuit. [2 pts]

(e) Calculate the quiescent point when β becomes 50% greater than the given value above and comment on the sensitivity of the circuit to the change in β. [2 pts]

(f) Find the voltage gain, input resistance, and output resistance values at the Q-point in question 3(d). [8 pts]

(g) Why is it necessary to operate the BJT in the active region for amplifier circuits? [3 pts]

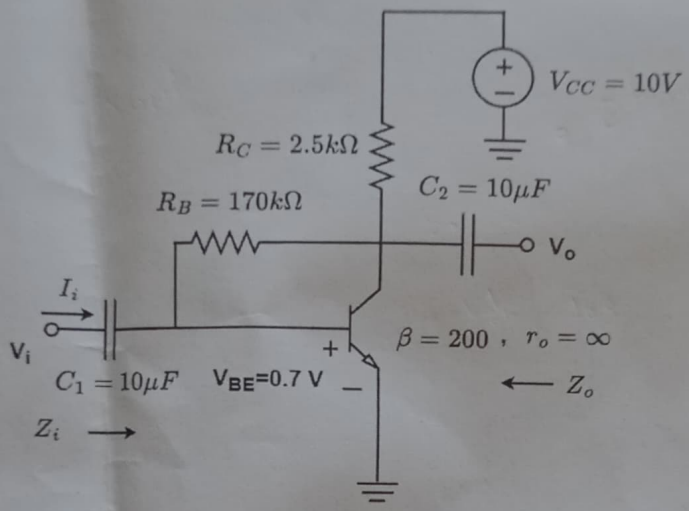

Fig. 3: Capacitively Coupled BJT Circuit for Q-II

Question IV: For the three circuits shown in Fig. 4, find the label node voltages and the operating region of BJTs. Assume that V_{BE}= 0.7 V. [6+6+6 Pts]

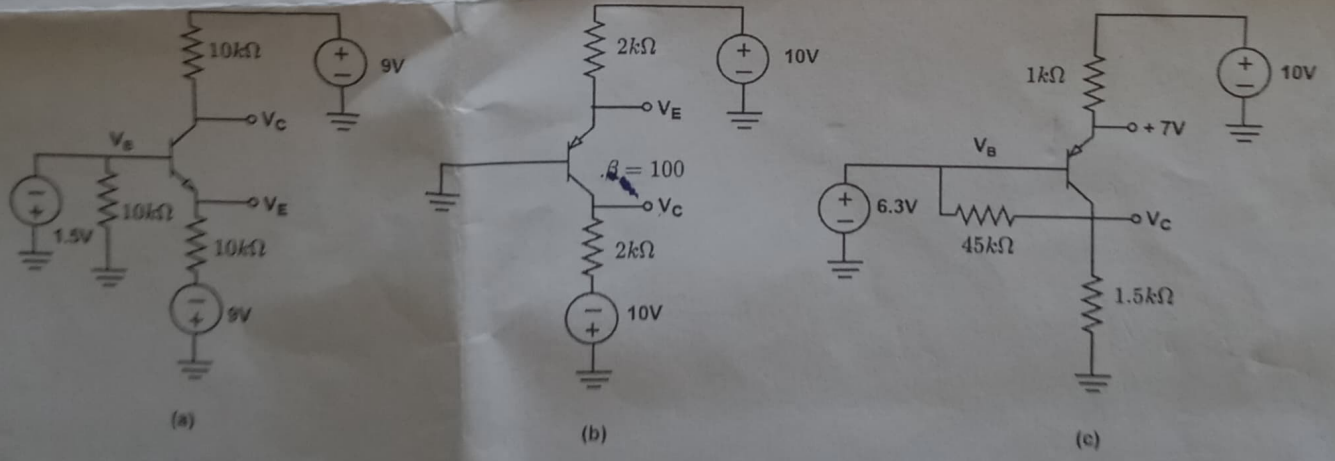

Fig. 4: DC-biased BJT Circuits for Q-IV

INDIAN INSTITUTE OF TECHNOLOGY ROPAR
GE108: Basic Electronics
End-Semester Examination

Max. Marks: 65 Duration: 3 Hours

Question I: Consider the circuit shown in Fig. 1 with three ideal op-amps and resistors. Given that $V_1 = 5$ V, $V_2 = 4.75$ V, $R_1 = 1$ kΩ, $R_2 = 49$ kΩ, $R_3 = 10$ kΩ and $R_4 = 10$ kΩ. Please find the output voltage (Vo) and justify the role of each op-amp configuration. [6+2 pts]

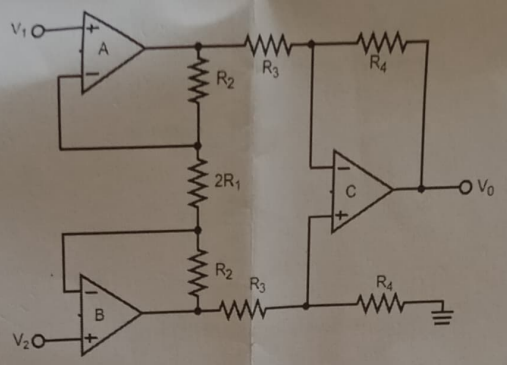

Fig.2: Circuit for Question-I

Question II: Consider the circuit shown below with three op-amps, two capacitors and six resistors. [8+2+2 pts]

(a) Calculate the overall transfer function (V_O/V_I).
(b) Explain the role of each op-amp configuration.
(c) Name the type of filter designed using the three-stage op-amp.

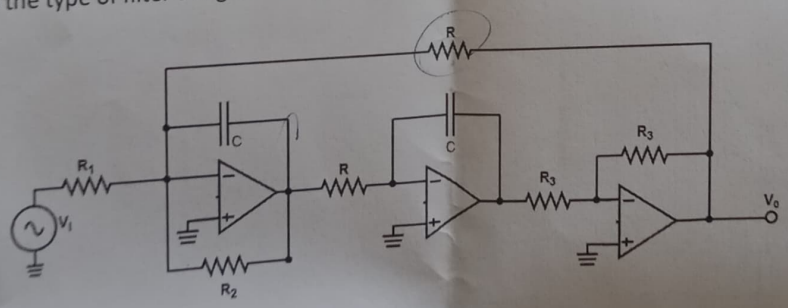

Fig.2: Circuit for Question-II

Question III: The MOSFET in the circuit of Fig. 3 has the following values: transconductance (g_m)=0.5 mA/V, drain-to-source current (I_{DS})=0.5 mA, $\mu_n C_{ox}$=12.5 μA/V^2, threshold voltage (V_{TH})= 1.5 V, and surface mobility of electrons $(\mu_n) = 450\ cm^2/V\text{-}s$. [2+3+4+4+4+3+3+4 pts]

(a) What is the name of the amplifier configuration?
(b) Find out V_D, V_S, and V_{GS} for below circuit?

(c) Plot the quiescent (Q) point position on the load line for the above circuit. Determine the maximum range of allowed input small signal voltage (Vsig) for this amplifier.

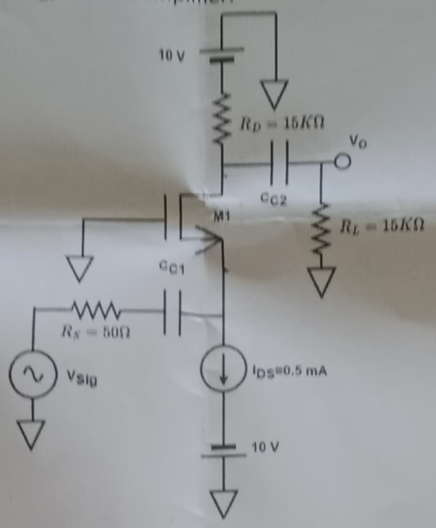

Fig. 3: Capacitively Couple MOSFET Circuit

(d) Find the input and output resistance in the circuit.
(e) Calculate the value of open-circuit voltage gain and overall voltage gain.
(f) Describe a practical use for this circuit and explain its suitability for that application.
(g) What is the role of I_{DS} current source in this circuit?
(h) What is the difference between the saturation regions in MOSFET and BJT?

Question IV: For the three circuits shown in Fig. 4, find the label node voltages, label current values, and the operating region of MOSFETs. The transistors are characterized by $\mu_n C_{ox}$=2.5 μA/V^2, $\mu_p C_{ox}$=20 μA/V^2, $V_{TH,n} = 1\ V$, $V_{TH,p} = -1\ V$, $(W/L)_n = (W/L)_p = 3$, and $\lambda_n = \lambda_p = 0$, where n and p indicate n-type and p-type MOSFETs. [6+6+6 pts]

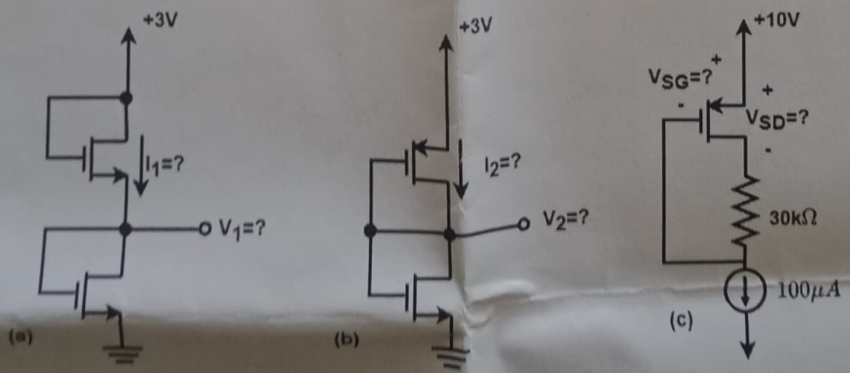

Fig. 4: DC-biased MOSFET Circuits